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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,557	07/24/2003	Shigeo Kigo	P23981	8098

7055 7590 10/27/2006

GREENBLUM & BERNSTEIN, P.L.C.  
1950 ROLAND CLARKE PLACE  
RESTON, VA 20191

EXAMINER

EISEN, ALEXANDER

ART UNIT PAPER NUMBER

2629

DATE MAILED: 10/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/625,557

Applicant(s)

KIGO ET AL.

Examiner

Alexander Eisen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 31 July 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 14-25 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 14-25 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date <u>8/23/06, 6/30/06</u> . | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 14-16 and 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanazawa, US 5,654,728 (reference of record).

With respect to claim 14 Kanazawa teaches a driving circuit that drives a display panel having an electrode, comprising a first switching element SW14 (in FIG. 4) that supplies a charge from a recovering capacitor C2 to the electrode Y1 of the display panel; an interconnector (a node where inductance L2 connects to the diodes D14 and D15) connected to said first switching element through a first one-way conductive element D14; a second switching element SW15 that recovers the charge from the electrode of the display panel to said recovering capacitor C2; a second one-way conductive element D15 provided between said second switching element and said interconnector; and a frequency reducer (protective diodes connected reversely and in parallel between the drains and sources of the switches-transistors SW14 and SW15) connected in parallel with said first switching element SW14, that is operable to reduce a resonance frequency of an LC resonance resulting from a parasitic capacitance of said first switching element, and an inductance component L2 of said interconnector, wherein the charge is supplied to the electrode of the display panel from said recovering capacitor through said first switching element and said interconnector.

While Kanazawa does not specifically teach that the diodes are frequency reducers, it is well within the knowledge and skills of those of ordinary skill in the art that the diodes possess such properties as capacitances, which if added to the parasitic capacitances of the switching elements would reduce the resonance frequency resulting from the parasitic capacitance of the switching element.

As pertaining to claim 15, Kanazawa teaches a frequency reducer (see the reasoning above in relevance to the first switch frequency reducer) connected in parallel with the second switching element SW15, that is operable to reduce a resonance frequency of an LC resonance resulting from a parasitic capacitance of said first switching element, and an inductance component L2 of said interconnector, wherein the charge is supplied to the electrode of the display panel from said recovering capacitor through said first switching element and said interconnector.

Claim 16 includes the limitations of preceding claims 14 and 15 and therefore is rejected on the same grounds.

As pertaining to claims 23-25 Kanazawa teaches a display device incorporating a driver (see title of Kanazawa), as presented in claims 14-16, and therefore these claims are rejected on the same grounds.

3. Claims 17-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanazawa in view of Lai, "Resonant Snubber-Based Soft-Switching Inverters for Electric Propulsion Drives" (submitted by the Applicant with IDS of 08/23/06).

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Kanazawa teaches all the limitations of the claims 17-22 except for the capacitor(s) connected in parallel with one of the first and second switches (transistors), or with the both switches.

Lai teaches a similar driver circuit arrangement (FIG. 3), wherein in addition to the diodes connected in parallel to the switches, taught by Kanazawa, capacitors  $C_r$  are also connected to the switches in parallel as lossless snubbers in order to allow a zero-voltage turn-off and to slow the voltage rise rate  $dv/dt$  (page 75, col. 2, lines related to *Mode 2* operation).

Hence, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to introduce the capacitors taught by Lai into the driving circuit of Kanazawa for the benefits taught by the latter, namely to reduce losses during turn-off and improve the voltage rate by slowing it down. Again, as it would be well known to those of ordinary skill in the art, introducing the capacitors into the switching circuit, as was suggested by Lai, would reduce the parasitic resonant frequency or the “ringing” of the latter, because the slower voltage rise rate would inevitably lead to reducing or eliminating of such oscillation.

#### ***Response to Arguments***

4. Applicant's arguments with respect to claims 14-25 have been considered but are moot in view of the new ground(s) of rejection.

#### ***Conclusion***

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

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A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

**Turney, US 4,495,445**, discloses using a parallel capacitor for reducing a parasitic resonant frequency.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander Eisen whose telephone number is (571) 272-7687. The examiner can normally be reached on M-F (9:00-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Alexander Eisen  
Primary Examiner  
Art Unit 2629

20-Oct-06